# Nolan Chu

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## Education

**Virginia Tech** — Blacksburg, VA
Master of Science in Computer Science (Thesis Track), **GPA:** 3.94/4.0 — Spring 2025 – Present
*Areas:* Computer architecture, hardware memory compression, digital hardware design
**Expected Graduation:** Fall 2026

**Virginia Tech** — Blacksburg, VA
Bachelor of Science in Computer Science, Minor in Mathematics, **GPA:** 4.0/4.0 — Fall 2022 – Winter 2024

**Selected Coursework:** Graduate Computer Architecture (BOOM/Chipyard, out-of-order cores, cache coherence); Compiler Optimizations; Advanced Parallel Computation; Computer Systems.

## Publication

**Nolan Chu**, Yoon Lee, Gagandeep Panwar, and Xun Jian. "Random-Access Hardware Sequence Compression." *Accepted to the 52nd International Symposium on Computer Architecture* (**ISCA 2026**).

Proposes RST, a hardware memory-compression algorithm and accelerator that shrinks per-page dictionaries to 128 B while matching Deflate-class compression ratios (3.4× geomean across 88 benchmarks). ASIC synthesis in 7 nm reports 18 ns per-block decompression latency vs. ∼140 ns under the state of the art—a 4× average (up to 8×) reduction in compressed-memory access latency and 15% average system performance improvement in full-system Gem5 simulation.

*IP disclosure approved:* "Randomly-Decompressible Hardware Sequence Compression" (co-inventor with X. Jian).

## Professional Experience

**Research Associate (Upcoming Co-op)**, *AMD Research & Advanced Development* — Jun – Dec 2026
Joining the compression research group under Lucian Petrica within AMD Research. Research direction builds on expertise in compression algorithm/hardware co-design developed through RST.

**Graduate Research Assistant**, *HEAP Lab, Virginia Tech* — Spring 2025 – Present
Designed compressor and decompressor microarchitectures for **RST**, a page-level sequence-compression engine for hardware-compressed memory; implemented in SystemVerilog and synthesized in a predictive 7 nm PDK (ASAP7). Evaluated RST via Gem5 full-system simulation on server-style workloads. Currently implementing an LZ codec targeting 300 MHz on a CXL FPGA prototype for hardware memory compression reliability research.

**Graduate Teaching Assistant**, *CS/ECE 5504, Virginia Tech* — Spring 2026
TA under Prof. Feng for graduate computer architecture. Designed rubrics and grading infrastructure for assignments spanning CPU performance, caches, Tomasulo's algorithm, pipeline scheduling, and Gem5 simulation.

**ASIC Engineer Intern**, *Cisco Systems, San Jose, CA* — May – Aug 2025
Developed **KView**, an internal visualization tool (video demo) for debugging functional verification sweeps on network switches. Built an automated Verilog design-partitioning flow for multi-FPGA emulation by parsing thousands of RTL files, constructing a hierarchical connectivity graph, and identifying cross-FPGA nets.

**NSF REU Fellow**, *CS Department, Virginia Tech* — May – Aug 2024
Awarded NSF funding for research in hardware-efficient memory compression, co-designing compression algorithms with memory-controller microarchitecture and optimizing RTL implementations.

## Research Presentations

- Presented RST to AMD Research (Lucian Petrica, Tobias Alonso Pugliese), Dec. 2025.
- VT Biweekly Memory Systems Reading Group, Dec. 2025.
- Samsung Memory Solutions Lab / VT Grant Meeting (PIs: X. Jian, S. H. Noh, H. Li), 2025.
- Invited presentation to Bill Starke, IBM Distinguished Engineer and Power Processor Chief Architect.
- VTURCS Research Symposium, poster presentation, Apr. 2024.

## Technical Skills

**Architecture:** Hardware memory compression, cache/memory hierarchy, branch prediction, OoO cores (BOOM), DRAM/memory controllers.
**Languages:** SystemVerilog, Verilog, C/C++, Python, Rust, RISC-V assembly.
**Tools:** Gem5, Chipyard/BOOM, Verilator, Synopsys Design Compiler, Cadence, Vivado, Git, Linux, LLVM.

## Awards & Honors

**CS Department Scholars Award** (2024); **VTHacks 11: 1st Place Overall** (LifeLens health data platform, 2023); **MCM Team Leader** (2023, 2024); **President's List** (2022–2024).